AMENDMENTS TO THE DRAWINGS

Attached please find four replacement drawings replacing FIGS. 9-12.

Attachment: Four (4) Replacement Sheets

REMARKS

Claims 1-14 have been examined. Claims 15-17 have been added. Claims 1-17 are all the claims pending in the application.

Allowable subject matter

Applicant thanks the Examiner for allowing claims 3, 5, and 8-9, and for indicating that claim 4 would also be allowable if rewritten to overcome the § 112 rejection discussed further below. Moreover, claim 6 is objected to as being dependent upon rejected independent claim 4, but would be allowable if rewritten in independent form. Applicant has amended claim 4, as discussed below, and accordingly requests the Examiner to allow claims 4 and 6.

Objections to the Drawings

Figures 8-12 stand objected to because the Examiner maintains they should be labeled "prior art" because only that which is old is illustrated. Applicant notes that Fig. 8 is already marked as "prior art". Applicant herewith submits four replacement drawings of Figs. 9-12, and respectfully requests the Examiner to accept the drawings in the next action.

Objections to the Claims & Claim rejections -- 35 U.S.C. § 112, first paragraph

Claim 11 stands objected to because of informalities. Specifically, the Examiner notes that "the" should be changed to "an". Moreover, claims 11-14 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant has amended claim 11 and therefore respectfully requests the Examiner to withdraw the rejection and allow claims 11-14.

Claim rejections -- 35 U.S.C. § 112, second paragraph

Claim 4 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant has herein amended claim 4 and respectfully requests the Examiner to withdraw the rejection and allow claim 4, and to accordingly remove the objection from and allow claim 6 which depends therefrom.

Claim rejections -- 35 U.S.C. § 103

Claims 1, 2, and 7 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishimura, which is already of record, in view of U.S. Patent No. 5,712,651 to Tomiyasu.

Applicant respectfully notes that the invention disclosed in the cited reference to Nishimura is equivalent to the prior art described, for example, in Figs. 9-11 of the present specification and drawings.

Applicant notes that in the Final Office Action, the Examiner has applied a new secondary reference to Tomiyasu, and asserts that Tomiyasu teaches the claim feature of converting input video data that is composed of parallel data into partially serialized output video data, as set forth, e.g., in claim 1. However, Applicant respectfully submits that Tomiyasu is no better than the reference to Thompson which was cited in the prior action. Specifically, the Examiner cites Fig. 3 as allegedly teaching the claimed feature. However, Applicant respectfully disagrees with the Examiner's position.

First, Tomiyasu is directed to a method and apparatus for grey-scale emulation for emulatively increasing the number of expressed gray scale levels for use with a color type TFT

LCD. See col. 1, lines 30-36. The invention disclosed by Tomiyasu thus has a goal of realizing the full-color display on the 16-gray-scale TFT color display device. This goal is completely different from that of the claimed invention.

Applicant respectfully submits that Tomiyasu merely discloses a combination of 16 gray scale levels expressed by the upper 4-bit data to 16 gray scale levels expressed by a frame rate controller. As described at col. 3, line 9 to col. 4, line 25, Tomiyasu adds "0001" to the upper significant bits of the video R, G, and B data using an adder 391. This adder, thus, acts as a shift register. For example, data of "0010" becomes "0011". This data is then fed into a multiplexer, and the newly shifted data or the original data is selected based on the lower 4 bits of the video data. See col. 9, lines 24-47. Frame rate controller 36 uses the lower 4 bits of the video R, G, and B data to select one of 16 different types of dither matrices. See col. 9, lines 50-55. The dither matrices are prepared to prevent flicker on the display screen.

Thus, Tomiyasu merely teaches selecting between a shifted video data and the next video data, and thus does not teach producing partially serialized output data from input video data composed of parallel data, as set forth by claim 1. Accordingly, Applicant respectfully submits that claim 1 is patentable over the Nishimura and Tomiyasu combination, and claim 7 is patentable based on its dependency.

Claim 2 recites the feature of serializing input video data of a 3 X 2^n-bit parallel in a 2^m-bit unit (n and m: natural numbers larger than zero, n > m) to produce output video data of a 3 X $2^{(n-m)}$-bit parallel. The Examiner maintains that Tomiyasu teaches this feature at Fig. 3. However, Tomiyasu teaches a 3 x 8 bit input parallel data. Thus, n=3. This data is in a 4 bit

unit. Thus, m=2. However, Tomiyasu teaches that the output data is 3 x 4 bit data. Thus, the claimed relationship $3 \times 2^{(n-m)}$ is not met. Applicant therefore respectfully submits that claim 2 is patentable over the Nishimura and Tomiyasu combination.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishimura in view of U.S. Patent No. 6,550,026 to Wright.

As an initial matter, one having skill in the art would not have been motivated to combine the Nishimura and Wright teachings. First, Nishimura is directed to drive circuits of a LCD display, whereas Wright is directed high speed test system for a memory device. Second, the Examiner maintains that motivation exists to reduce the number of compare circuits. See Wright, col. 3, lines 32-35. However, reducing the number of circuit components is not a stated or implied problem with which Nishimura is concerned. Moreover, Wright is concerned with reducing the number of compare circuits *in on-chip test circuitry* (see col. 3, lines 34-35), whereas Nishimura is not directed at test circuitry. Therefore, for these reasons, Applicant respectfully submits that one having skill in the art would not look to combine the teachings of Wright and Nishimura.

Since neither Nishimura nor Wright, standing alone, teach all of the features of claims 10-12, claims 10-12 are patentable.

With further regard to claim 11, claim 11 recites the feature of a second comparator which is configured to compare "said first bits which are not delayed by said delay circuit with said second bits". The Examiner acknowledges that Nishimura does not teach this feature. Thus, the Examiner argues that Wright discloses comparing odd numbered bits with even

numbered bits, and that one having ordinary skill would combine this teaching with Nishimura to "increase the speed of data comparison". However, the Examiner has provided no motivation for specifically adding a second comparator in addition to the first comparator, or one that compares bits with are not delayed with second bits. Moreover, Applicant respectfully submits that adding a second comparator would add computation time and accordingly take longer to compress the data. Accordingly claim 11 is patentable for these reasons.

Claims 13-14 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishimura in view of Wright, in further view of Tomiyasu. Applicant respectfully submits that claims 13-14 are patentable based on their respective dependencies.

New claims

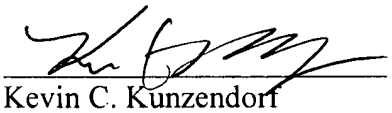
Applicant herein adds new claims 15-17 and submits that they are patentable based on their dependencies.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Kevin C. Kunzendorf
Registration No. 58,308

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
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